<center>REMARKS/ARGUMENTS</center>

Claims 27, 29-38, and 40-58 are pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of these remarks.

<u>Improper Finality</u>

The finality of the pending office action is improper. In the previous, final office action dated 5/22/07, the Examiner rejected claims 27, 29-31, 34-38, 40-42, and 45-52 under 35 U.S.C. 103(a) as being unpatentable over Dokic in view of Hughes-Hartogs. In the Response filed on 7/16/07, the Applicant argued that claims 27, 29-31, 34-38, 40-42, and 45-52 were allowable over Dokic in view of Hughes-Hartogs and that the rejections of those claims under 35 U.S.C. 103(a) were improper. Significantly, in response to that previous, final office action, the Applicant did <u>not</u> amend <u>any</u> of the claims.

In the present office action, the Examiner applied new grounds of rejection to claims 27, 29-31, 34-38, 40-42, and 45-52. In particular, claims 27, 29-30, 34, 36-38, 40-42, 45, and 47-51 were rejected under 35 U.S.C. 102(e) as being anticipated by Lindberg; claims 31 and 52 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lindberg in view of Tyrell; and claim 35 was rejected under 35 U.S.C. 103(a) as being unpatentable over Lindberg in view of Russell.

In paragraph 22 of the pending office action, the Examiner stated that "Applicant's amendment on 2/22/07 necessitated the new ground(s) of rejection presented in this Office action." However, the Applicant's amendment of 2/22/07 was filed in response to the office action dated 11/15/06, <u>not</u> in response to the previous office action dated 5/22/07. Since the new grounds of rejection were <u>not</u> necessitated by any amendments to the claims made in response to the previous office action, the finality of the pending office action is improper and should be withdrawn.

<u>Allowable Subject Matter and Claim Rejections</u>

In paragraph 3 of the final office action, the Examiner objected to claims 32-33 and 43-44 as being dependent upon rejected base claims, but indicated that those claims would be allowable if rewritten in independent form. In paragraph 4, the Examiner allowed claims 53-58. In paragraph 5, the Examiner rejected claims 27, 29-30, 34, 36-38, 40-42, 45, and 47-51 under 35 U.S.C. 102(e) as being anticipated by Lindberg. In paragraph 15, the Examiner rejected claims 31 and 52 under 35 U.S.C. 103(a) as being unpatentable over Lindberg in view of Tyrell. In paragraph 18, the Examiner rejected claim 35 under 35 U.S.C. 103(a) as being unpatentable over Lindberg in view of Russell. For the following reasons, the Applicant submits that all of the pending claims are allowable.

According to claim 38, the first processor (i) generates a data word having two or more data bits, wherein each data bit has either a first bit value or a second bit value, and (ii) transmits the data word from a data port of the first processor to the signal unit. The signal unit (i) converts the data word into two or more interrupt signals by analyzing the bit value of each of two or more data bits in the data word, wherein each analyzed data bit in the data word having a specified bit value corresponds to a different interrupt signal, and (ii) transmits each interrupt signal from the signal unit to an interrupt port of an other processor. The Applicant submits that the cited references do not teach or even suggest such a combination of features.

In paragraph 12, the Examiner stated that claim 38 was rejected for the same reasons as stated in the rejection of claim 27. In rejecting claim 27, in paragraph 6, the Examiner cited Lindberg's Fig. 4 as an example of the invention of claim 27. For the following reasons, the Applicant submits that the Examiner mischaracterized the teachings of Lindberg in rejecting both claims 27 and 38.

Lindberg's Fig. 4 shows a fault tolerant switching system 100 comprising switching network terminals (SNTs) 102, 104, 140, 150, multiplexing devices (MUX) 114, 116, switches 118, 120 or equivalents, demultiplexing devices (DEMUX) 128, 130, and physical links that interconnect those elements. See, e.g., column 5, lines 58-66. Switching system 100 has a redundant architecture comprising two switching planes: plane A and plane B. See, e.g., column 6, lines 29-30.

Each incoming SNT 102, 104 receives and distributes an input data signal to both mux 114 of switching plane A and mux 116 of switching plane B. See, e.g., column 6, line 58, to column 7, line 6. Each mux 114, 116 multiplexes the two received data signals to generate a single output data signal for transmission to the corresponding switch 118, 120. See, e.g., column 7, lines 6-18. Each switch 118, 120 switches the corresponding received data signal for transmission to the corresponding demux 128, 130. See, e.g., column 7, lines 18-22. Each demux 128, 130 demultiplexes the corresponding received data stream into two data signals, one of which is transmitted to outgoing SNT 140 and the other to outgoing SNT 150. See, e.g., column 7, lines 22-29.

Each outgoing SNT 140, 150 receives two serial streams of data: one from switching plane A and the other from switching plane B. See, e.g., column 7, lines 30-32. Each outgoing SNT 140, 150 analyzes the two received streams of data to (1) detect the presence of line code errors and lost frame alignments in the corresponding switching planes and (2) set corresponding control signals accordingly. See, e.g., column 7, line 34, to column 8, line 22. Each outgoing SNT 140, 150 uses those control signals to generate a corresponding non-redundant output data signal. See, e.g., column 8, lines 23-26.

None of this has anything to do with interrupt signals. The term "interrupt signal" is an extremely well-known term that would be readily understood by those of ordinary skill in the art. In the context of claim 38, an interrupt signal transmitted between two processors (also called an "inter-processor interrupt") is a signal transmitted from one processor to interrupt (e.g., stop) the processing implemented by another processor in a multi-processor system. See, e.g., Wikipedia definition of "inter-processor interrupt."

According to the Examiner's reasoning in paragraph 6 and referring to elements in Lindberg's Fig. 4:

o   SNT 102 is supposed to be an example of the first processor of claim 38;

o   Demux 130 is supposed to be an example of the signal unit of claim 38; and

o   SNT 102, demux 128, and SNT 140 are supposed to be examples of the one or more other processors of claim 38.

The Applicant submits that the Examiner's mapping of claim 38 onto the cited elements in Lindberg's Fig. 4 does not satisfy the explicit recitations of claim 38.

According to claim 38, the first processor (i) generates a data word having two or more data bits, wherein each data bit has either a first bit value or a second bit value, and (ii) transmits the data word

from a data port of the first processor to the signal unit. It is true that Lindberg's SNT 102 transmits data words that are eventually received at demux 130 (albeit, after passing through mux 116 and switch 120).

According to claim 38, the signal unit (i) converts the data word into two or more interrupt signals by analyzing the bit value of each of two or more data bits in the data word, wherein each analyzed data bit in the data word having a specified bit value corresponds to a different interrupt signal, and (ii) transmits each interrupt signal from the signal unit to an interrupt port of an other processor.

First of all, Lindberg's demux 130 does not convert a data word received from SNT 130 into two or more interrupt signals. At most, Lindberg's demux 130 demultiplexes the single data signal received from switch 120 into two (or more) data signals. The signals transmitted from demux 130 are not interrupt signals; they are data signals. Significantly, demux 130 does not analyze the bit value of different data bits in a data word of its single received data signal, where each analyzed data bit corresponds to a different interrupt signal.

Nor does Lindberg's demux 130 transmit any signal to an interrupt port of an other processor. First of all, in terms of the Examiner's mapping, demux 130 does not transmit any signals to SNT 102 or demux 128. Lindberg's demux 130 does transmit signals to SNT 140 and SNT 150, but those signals are not interrupt signals transmitted to interrupt ports of SNT 140 and SNT 150. Rather, demux 130 transmits one data signal to serial-to-parallel (S2P) converter 162 in SNT 150 and another data signal to an analogous S2P converter in SNT 140 (see, e.g., column 7, lines 64-67), but those S2P converters do not represent or correspond to interrupt ports of SNT 140 and SNT 150. Just because Lindberg's serial-to-parallel converters convert serial data into parallel data, that does not mean that the converted data corresponds to interrupt signals.

For all these reasons, the Applicant submits that currently amended claim 38 is allowable over Lindberg. For similar reasons, the Applicant submits that currently amended claims 27, 49, and 51 are allowable over Lindberg.

Since claims 29-37 depend directly or indirectly from claim 27, it is further submitted that those claims are also allowable over Lindberg. Since claims 40-48 depend directly or indirectly from claim 38, it is further submitted that those claims are also allowable over Lindberg. Since claim 50 depends from claim 49, it is further submitted that claim 50 is also allowable over Lindberg. Since claim 52 depends from claim 51, it is further submitted that claim 52 is also allowable over Lindberg.

In view of the above remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Fees

During the pendency of this application, the Commissioner for Patents is hereby authorized to charge payment of any filing fees for presentation of extra claims under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17 or credit any overpayment to Mendelsohn & Associates, P.C. Deposit Account No. 50-0782.

The Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Respectfully submitted,

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